Amendments to the Claims:

This listing of claims will replace all prior listing of claims in the application.

Listing of Claims:

1. (Currently Amended) A ~~Nonvolatile~~ nonvolatile semiconductor storage element ~~with~~ comprising: a semiconductor substrate ~~(1) in which~~ having a source region ~~(S)~~, a drain region ~~(D)~~ and an intermediate channel region ~~are formed~~;

a control layer ~~(5) which is formed~~ on a first ~~part section (I)~~ portion of the channel region and ~~is~~ insulated ~~from this~~ therefrom by a first insulating layer ~~(2A)~~;

a charge storage layer ~~(3A, 3B) which is formed~~ on a second ~~part section (IIA, IIB)~~ portion of the channel region and ~~is~~ insulated ~~from that~~ therefrom by a second insulating layer ~~(2BA, 2BB)~~; ~~and~~

a programming layer ~~(6A, 6B) which is formed~~ on the charge storage layer ~~(3A, 3B)~~ and ~~is~~ insulated ~~from that~~ therefrom by a third insulating layer ~~(4A, 4B), characterized by~~; and

an interconnect layer ~~(6AA, 6BB)~~ for electrically connecting the programming layer ~~(6A, 6B)~~ to the source region ~~(S)~~ or drain region ~~(D)~~, wherein the second ~~part section~~ portion of the channel region has a source side ~~part section (IIB)~~ and a drain side ~~part section (IIA);~~

wherein the charge storage layer has a source side charge storage layer ~~(3B)~~ and a drain side charge storage layer, ~~(3A);~~

wherein the programming layer has a source side programming layer ~~(6B)~~ and a drain side programming layer ~~(6A)~~; and wherein the interconnect layer has a source side interconnect layer ~~(6BB)~~ and a drain side interconnect layer ~~(6AA)~~, the source side interconnect layer ~~(6BB)~~ electrically connecting the source side programming layer ~~(6B)~~ to the source region ~~(S)~~ and the drain side interconnect layer ~~(6AA)~~ electrically connecting the drain side programming layer ~~(6A)~~ to the drain region ~~(D)~~.

2. (Currently Amended) The ~~Nonvolatile~~ nonvolatile semiconductor storage element according to Claim 1, ~~characterized in that~~ wherein the charge storage layer ~~(3A, 3B) represents~~ comprises an electrically nonconductive layer.

3. (Currently Amended) The ~~Nonvolatile~~ nonvolatile semiconductor storage element according to ~~either of Claims~~ Claim 1 ~~and 2, characterized in~~ that, wherein the first and second insulating layers ~~layer (2A, 2BA, 2BB) exhibits~~ comprise SiO_2.

4. (Currently Amended) The ~~Nonvolatile~~ nonvolatile semiconductor storage element according to ~~one of Claims~~ Claim 1 ~~to 3, characterized in that~~ wherein the charge storage layer ~~(3A, 3B) exhibits~~ comprises one of an Si_3N_4, HFO_2 or ZrO_2 layer.

5. (Currently Amended) The ~~Nonvolatile~~ nonvolatile semiconductor storage element according ~~to one of Claims~~ Claim 1 ~~to 4, characterized in that~~ wherein the control layer ~~(5)~~, the programming layer, ~~(6A, 6B)~~ and the interconnect layer ~~(6AA, 6BB) have~~ comprise doped polysilicon.

6. (Currently Amended) A ~~Method~~ method for producing a nonvolatile semiconductor storage element ~~with~~ comprising the ~~following~~ steps of:

a) preparing a semiconductor substrate ~~(1)~~ having a surface;

b) forming a first insulating layer ~~(2A)~~ on the surface of the semiconductor substrate ~~(1)~~;

c) forming and patterning a control layer ~~(5)~~ on the surface of the first insulating layer ~~(2A)~~;

d) forming a sequence of layers ~~consisting of~~ including a second insulating layer ~~(2B)~~, a charge storage layer, ~~(3)~~ and a third insulating layer ~~(4)~~ on the surface of the semiconductor substrate ~~(1)~~ and ~~of~~ the patterned control layer ~~(5)~~;

e) forming and patterning a programming layer ~~(6A, 6B)~~ on the third insulating layer ~~(4)~~ on the side walls of the ~~patterned~~ control layer ~~(5)~~;

f) forming source regions ~~(S)~~ and drain regions ~~(D)~~ in the semiconductor substrate ~~(1) by~~ using the ~~patterned~~ programming layer ~~(6A, 6B)~~ and the patterned control layer ~~(5)~~ as a mask;

g) patterning the third insulating layer ~~(4)~~, the charge storage layer, ~~(3)~~ and the second insulating layer ~~(2B) by~~ using the ~~patterned~~ programming layer ~~(6A, 6B)~~ as a mask;

h) forming a fourth insulating layer ~~(7)~~ on the surface of the semiconductor substrate ~~(1)~~, ~~of~~ the patterned programming layer ~~(6A, 6B)~~ and ~~of~~ the patterned control layer ~~(5)~~;

i) exposing interconnect areas in at least portions of ~~parts of~~ the patterned programming layer ~~(6A, 6B)~~, ~~of~~ the source region, ~~(S)~~ and ~~of~~ the drain region ~~(D)~~; and

j) forming an electrically conductive interconnect layer ~~(6AA, 6BB)~~ in the ~~exposed~~ interconnect areas ~~for contacting~~ that contact the programming layer ~~(6A, 6B) of~~ overlying the source region ~~(S)~~ and overlying ~~of~~ the drain region ~~(D)~~.

7. (Currently Amended) The ~~Method~~ method according to Claim 6, ~~characterized in that a gate dielectric is formed as~~, wherein forming the first insulating layer ~~(2A) in step b)~~ comprises forming a gate dielectric layer.

8. (Currently Amended) The ~~Method~~ method according to Claim 6 ~~or 7~~, ~~characterized in that a first polysilicon layer is deposited as~~, wherein forming a control layer comprises forming a first polysilicon layer ~~(5) in step c)~~.

9. (Currently Amended) The ~~Method~~ method according to ~~one of Claims~~ Claim 6 ~~to 8, characterized in that an ONO~~, wherein forming a sequence of layers comprises forming an oxide layer, a nitrile layer, and an oxide layer. ~~is deposited in step d).~~

10. (Currently Amended) The ~~Method~~ method according to ~~one of Claims~~ Claim 6 ~~to 9, characterized in that a spacer method is performed for~~, wherein depositing and patterning a ~~second polysilicon layer as~~ programming layer ~~(6A, 6B) in step e)~~ comprises depositing a polysilicon layer and patterning the polysilicon layer to form sidewall spacers on the control layer.

11. (Currently Amended) The ~~Method~~ method according to ~~one of Claims~~ Claim 6 ~~to 10, characterized in that an~~, wherein forming source regions and drain regions comprises ion implantation and a thermal post-treatment ~~is performed~~ for diffusing-out and activating the source and drain regions ~~(S, D) in step f)~~.

12. (Currently Amended) The ~~Method~~ method according to ~~one of Claims~~ claim 6 ~~to 11~~, ~~characterized in that an anisotropic~~ further comprising anisotropically

dry etching ~~of~~ the sequence of layers and ~~an isotropic~~ isotropically etching-back ~~of~~ at least the charge storage layer ~~(3) is performed for forming~~ to form charge storage layer recesses ~~in step g)~~.

13. (Currently Amended) The ~~Method~~ method according to Claim 12, ~~characterized in that~~, wherein forming a fourth insulating layer comprises depositing an oxide ~~deposition is performed for filling up~~ to fill the charge storage layer recesses ~~in step h)~~.

14. (Currently Amended) The ~~Method~~ method according to ~~one~~ of ~~Claims~~ Claim 6 ~~to 13, characterized in that~~, wherein forming an electrically conductive interconnect layer comprises depositing and planarizing a third polysilicon layer ~~is deposited and planarized as interconnect layer (6AA, 6BB) in step j)~~.

15. (Currently Amended) A ~~Method~~ method for writing an information item into a nonvolatile semiconductor storage element configured according to ~~one of Claims~~ Claim 1 ~~to 5~~, ~~with~~ comprising the following steps:

a) applying a first positive write voltage to the source side interconnect layer ~~(6BB)~~;

b) applying a second positive write voltage, which is much higher than the first positive write voltage, to the drain side interconnect layer ~~(6AA)~~; and

c) applying a third positive write voltage, which is slightly higher than an ~~the~~ RMS threshold voltage of a respective inner transistor, to the control layer ~~(5)~~ for generating an SSI condition.

16. (Currently Amended) A ~~Method~~ method for erasing an information item in a nonvolatile semiconductor storage element configured according to ~~one of Claims~~ Claim 1 ~~to 5~~, comprising the ~~following~~ steps of:

a) applying a floating potential to the source side interconnect layer ~~(6BB)~~;

b) applying a high first erase voltage to the drain side interconnect layer ~~(6AA)~~; and

c) applying a second erase voltage, which is lower than ~~the~~ an RMS threshold voltage of a respective inner transistor, to the control layer ~~(5)~~ for generating an avalanche effect condition.

17. (Currently Amended) A ~~Method~~ method for reading an information item in a nonvolatile semiconductor storage element configured according to ~~one of Claims~~ Claim 1 ~~to 5~~, comprising the ~~following~~ steps of:

a) applying a first positive read voltage to the source side interconnect layer ~~(6BB)~~;

b) applying a second read voltage, which is sufficiently smaller than the first read voltage, to the drain side interconnect layer ~~(6AA)~~; and

c) applying a third read voltage, which ~~is in the region of~~ has a magnitude similar to the first read voltage, to the control layer ~~(5)~~ for generating a reverse readout.